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EXAMINER	
LEWIS, MONICA	
ART UNIT	PAPER NUMBER
2894	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,961	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Monica Lewis	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-128* is/are pending in the application.

4a) Of the above claim(s) *88-94,96-105 and 115* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *88,95,106-109,111-114,116-123 and 125-128* is/are rejected.

7)☒ Claim(s) *110 and 124* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed February 16, 2009.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/16/09 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 88, 95, 106-109, 111-114, 116-123 and 125-128 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 88, 95 and 116-119 are rejected under 35 U.S.C. 103(a) as obvious over Sugiyama et al. (U.S. Patent No. 5,753,536) in view of Watanabe et al. (Japanese Patent No. 408017962).

In regards to claim 88, Sugiyama et al. ("Sugiyama") discloses the following:

a) a first substrate (10) comprising a first surface having interconnect contacts formed thereon (For Example: See Figure 16B); and

b) a second substrate (13) comprising a first surface having interconnect contacts formed thereon, a thermal diffusion bond between the first surface of the second substrate and the first surface of the first substrate that forms conductive paths between the interconnect contacts of the first surfaces of the first and second substrates, the first surface of the second substrate overlapping at least a majority of the first surface of the first substrate (For Example: See Figure 16B and Column 19 Lines 21-27).

In regards to claim 88, Sugiyama fails to disclose the following:

a) the first substrate is at least twice as thick as the second substrate.

However, Watanabe et al. ("Watanabe") discloses a first substrate that is at least twice as thick as the second substrate (For Example: See Paragraph 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include a first substrate that is at least twice as thick as the second substrate as disclosed in Watanabe because it aids in not producing a defect of operation (For Example: See Paragraph 9).

Additionally, since Sugiyama and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Sugiyama.

In regards to claims 95 and 119, Sugiyama fails to disclose the following:

a) at least one additional thinned substrate having circuitry formed thereon.

However, Leedy discloses at least one additional thinned substrate having circuitry formed thereon (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include at least one additional thinned substrate having circuitry formed thereon as disclosed in Leedy because it aids in providing a structural integrity (For Example: See Column 5 Lines 62-68 and Column 6 Line 15).

Additionally, since Sugiyama and Leedy are both from the same field of endeavor, the purpose disclosed by Leedy would have been recognized in the pertinent art of Sugiyama.

b) a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent thinned substrates.

However, Leedy discloses at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent thinned substrates (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent thinned substrates as disclosed in Leedy because it aids providing a structural integrity (For Example: See Column 5 Lines 62-68 and Column 6 Line 15).

Additionally, since Sugiyama and Leedy are both from the same field of endeavor, the purpose disclosed by Leedy would have been recognized in the pertinent art of Sugiyama.

c) conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated structure.

However, Leedy discloses conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated structure (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated structure as disclosed in Leedy because it aids providing a structural integrity (For Example: See Column 5 Lines 62-68 and Column 6 Line 15).

Additionally, since Sugiyama and Leedy are both from the same field of endeavor, the purpose disclosed by Leedy would have been recognized in the pertinent art of Sugiyama.

In regards to claim 116, Sugiyama discloses the following:

a) a first substrate having topside and bottomside surfaces, the topside surface of the first substrate having interconnect contacts formed thereon (For Example: See Figure 16B);

b) a second substrate having topside and bottomside surfaces, the bottomside surface of the second substrate having interconnect contacts formed thereon (For Example: See Figure 16B);

c) a thermal diffusion bond between the bottomside surface of the second substrate and the topside surface of the first substrate (For Example: See Figure 16B); and

d) conductive paths formed between the interconnect contacts on the topside of the first substrate and the bottomside of the second substrate, the conductive paths providing electrical connections between the first substrate and the second substrate, the bottomside surface of the second substrate overlapping at least a majority of the topside surface of the first substrate (For Example: See Figure 16B).

In regards to claim 116, Sugiyama fails to disclose the following:

a) the first substrate is at least twice as thick as the second substrate.

However, Watanabe discloses a first substrate that is at least twice as thick as the second substrate (For Example: See Paragraph 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include a first substrate that is at least twice as thick as the second substrate as disclosed in Watanabe because it aids in not producing a defect of operation (For Example: See Paragraph 9).

Additionally, since Sugiyama and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Sugiyama.

In regards to claim 117, Sugiyama discloses the following:

a) selected ones of said interconnect contacts on said topside surface are in electrical contact with selected ones of the interconnect contacts on said bottomside of said second substrate so as to form said electrical connection (For Example: See Figure 16B).

In regards to claim 118, Sugiyama discloses the following:

a) a first substrate having a first and second surface (For Example: See Figure 16B);

b) a second substrate having a first and second surface, wherein said second surfaces of the first and second substrates are opposite to said first surfaces (For Example: See Figure 16B);

c) a thermal diffusion bond between the bottomside surface of the second substrate and the topside surface of the first substrate (For Example: See Figure 16B); and

d) conductive paths formed on the first surfaces of the first and second substrates, the first surface of the second substrate overlapping at least a majority of the first surface of the first substrate (For Example: See Figure 16B).

In regards to claim 118, Sugiyama fails to disclose the following:

a) the first substrate is at least twice as thick as the second substrate.

However, Watanabe discloses a first substrate that is at least twice as thick as the second substrate (For Example: See Paragraph 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include a first substrate that is at least twice as thick as the second substrate as disclosed in Watanabe because it aids in not producing a defect of operation (For Example: See Paragraph 9).

Additionally, since Sugiyama and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Sugiyama.

6. Claims 106-108, 111-114, 120-122 and 125-128 are rejected under 35 U.S.C. 103(a) as obvious over Sugiyama et al. (U.S. Patent No. 5,753,536) in view of Leedy (U.S. Patent No. 5,354,695), Faris (U.S. Patent No. 5,786,629) and Sakui et al. (U.S. Patent No. 5,615,163).

In regards to claims 106 and 120, Sugiyama fails to disclose the following:

a) at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon.

However, Faris discloses at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon (For Example: See Column 3 Lines 60-63, Column 7 Lines 8-13 and Column 12 Lines 5-10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having

memory circuitry formed thereon as disclosed in Faris because it aids in providing parallel data processors (For Example: See Column 3 Lines 60-63).

Additionally, since Sugiyama and Faris are both from the same field of endeavor, the purpose disclosed by Faris would have been recognized in the pertinent art of Sugiyama.

b) a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines.

However, Sakui et al. ("Sakui") discloses a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couple the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines (For Example: See Figure 10, Column 5 Lines 20-67 and Column 6 Lines 1-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines as disclosed in Sakui because it aids in providing a means for saving the efficiency of a defective bit (For Example: See Column 5 Lines 11-18 and Column 6 Lines 40-63).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

c) a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment.

However, Sakui discloses a gate line selection circuit (22, 23, 24 and 22') that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

d) controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

However, Sakui discloses controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell

to couple a data value to one of the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 107 and 121, Sugiyama fails to disclose the following:

a) the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data

lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 108 and 122, Sugiyama fails to disclose the following:

a) programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 111 and 125, Sugiyama fails to disclose the following:

a) logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

However, Sakui discloses logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary

skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 112 and 126, Sugiyama fails to disclose the following:

a) the controller substrate logic is further configured to: prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 113 and 127, Sugiyama fails to disclose the following:

a) the controller substrate logic is further configured to prevent the use of at least one defective gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

In regards to claims 114 and 128, Sugiyama fails to disclose the following:

a) the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

However, Sakui discloses that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Sugiyama and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Sugiyama.

7. Claims 109 and 123 are rejected under 35 U.S.C. 103(a) as obvious over Sugiyama et al. (U.S. Patent No. 5,753,536) in view of Leedy (U.S. Patent No. 5,354,695), Faris (U.S. Patent No. 5,786,629), Sakui et al. (U.S. Patent No. 5,615,163) and Daberko (U.S. Patent No. 5,787,445).

In regards to claims 109 and 123, Sugiyama fails to disclose the following:

a) the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

However, Daberko discloses that the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell (For Example: See Abstract, Column 3 Lines 66 and 67, Column 4 Lines 1-11, Column 5 Lines 63-67 and Column 6 Lines 1-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sugiyama to include that an array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell as disclosed in Daberko because it aids in providing direct manipulation of data segments (For Example: See Column 3 Lines 60-64).

Additionally, since Sugiyama and Daberko are both from the same field of endeavor, the purpose disclosed by Daberko would have been recognized in the pertinent art of Sugiyama.

Allowable Subject Matter

8. Claims 110 and 124 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

/Monica Lewis/
Primary Examiner, Art Unit 2894

April 23, 2009